ABSTRACT OF THE DISCLOSURE

A trench isolation method for a semiconductor device, wherein a capping layer formed of an insulating material fills a recess generated at a border edge between an active area and an inactive area. The border edge is defined by a trench filled with insulating material. Filling the recess suppresses defects of the semiconductor device. Reduction of the isolating ability, due to the formation of gate poly residue during the forming of a gate, is prevented. Reduction of the threshold voltage of a transistor, caused by electric field concentration due to the gate poly residue, is suppressed. An oxide layer is also provided which protects an nitride pad during a plasma process.